REMARKS

1. Objections to the Drawings.

The Office Action of May 26, 2006 states that Applicant's claim is rejected pursuant to 37 C.F.R. §1.83(a) is required because the final transfer function calculated in the last step of claim 1 must be shown. Applicant cancels claim 1 thus resolving this objection. Also, the figures filed in the application are informal and the addition of reference numbers will to the objected figures will be added prior to allowance.

2. Objection Based on Double Patenting.

Applicant has deleted claim 1 and added new claims 2 - 35. Applicant's amendment should resolve the examiner's double patenting issue.

3. Application Is Rejected Based on 35 U.S.C. §101.

Applicant has deleted claim 1 and added new claims 2-35. Applicant's amendment should resolve the examiner's rejection based on 35 U.S.C. §101.

4. Application Is Rejected Based on 35 U.S.C. §112.

Applicant has deleted claim 1 and added new claims 2 – 35. Applicant's amendment should resolve the examiner's rejection based on 35 U.S.C. §112.

5. Application Is Rejected Based in 35 U.S.C. §103(a).

Claim 1 stands rejected pursuant to 35 U.S.C. §103(a) over the Kim et al. reference "Full Software Analysis and Impedance Matching of Radio Frequency CMOS Integrated Circuits" in view of the Lathi reference "Linear Systems and Signals." However, the combination of both of these references fail to teach applicant's invention. The Kim reference teaches the use of an impedance mismatch involving a full simulation of the entire integrated circuit using SPICE simulations (Kim Abstract). The Lathi reference teaches a treatise explanation of transfer functions. Nowhere in the references is there a suggestion to combine the two references to render obvious the Applicant's invention.

The Kim reference teaches a technique for using a SPICE simulation to obtain impedance mismatches. SPICE is a circuit level simulator that solves the entire system simultaneously and does not have higher levels of abstractions. All the impedance mismatch calculations are performed on the circuit level. As previously stated, the Lathi reference is a treatise on transfer functions. Previous attempts to calculate impedance mismatch were limited to circuit level components or circuit level components for entire systems. Calculations using SPICE, while accurate were extremely time consuming.

The Applicant's invention calculates impedance mismatch in a data flow simulation by decoupling the impedance mismatches that are solved during the simulation. A source block is not analyzed on a circuit level but on a higher level of abstraction. Where SPICE would calculate the impedance mismatch on circuit components, the Applicant's invention treats source blocks as higher functional components such as a transmitter or a receiver. The Applicant's disclosure teaches the determination of impedance mismatches without the need for a time consuming SPICE simulation.

The Applicant's use DSP techniques to represent the source block as for example a digital filter. In the data flow simulation, data is passed through the source block such that an impedance mismatch can be calculated that is accurate enough in a short time duration without having to complete the entire circuit level impedance mismatch for the complete system. In many higher level of abstraction simulations, the Applicant's disclosure teaches techniques that could provide impedance mismatch solutions in less than a second, where a SPICE calculation of the impedance mismatch, may take weeks, if ever, to solve.

CONCLUSION

In view of this Amendment, Applicant believes the new claims are now in condition for allowance. If for any reason the Examiner finds the Application other than in condition for allowance, the Examiner is respectfully requested to call the undersigned at (949) 337-0568 to discuss the steps necessary for placing the Application in condition for allowance.

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By:

Robert P. Hart
Registration No. 35,184
Law Offices of Robert P. Hart
28 East Jackson Building
10th Floor, Suite H528
Chicago, IL 60604
(949) 337-0568
(312) 264-2547 Fax